

Fig. 1A
SIDE VIEW

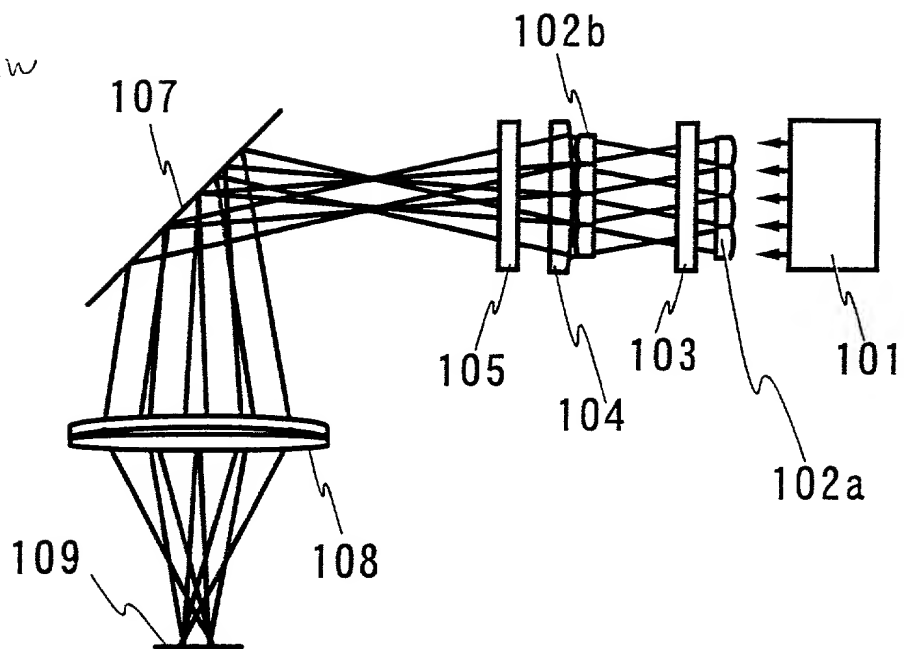
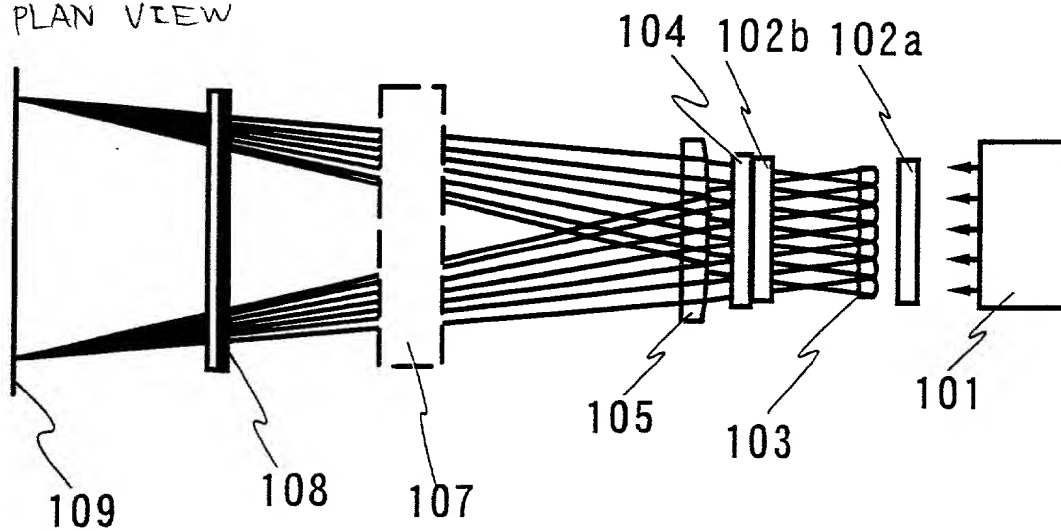


Fig. 1B
PLAN VIEW



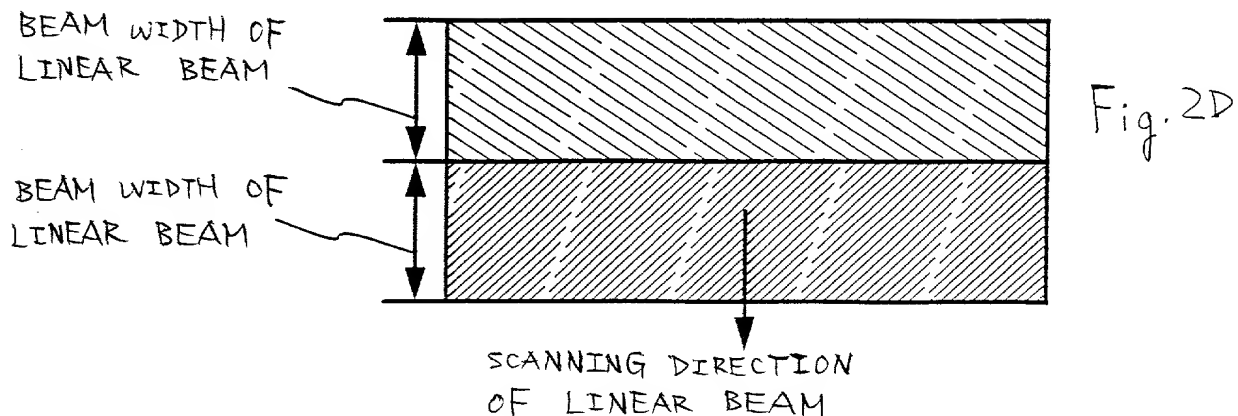
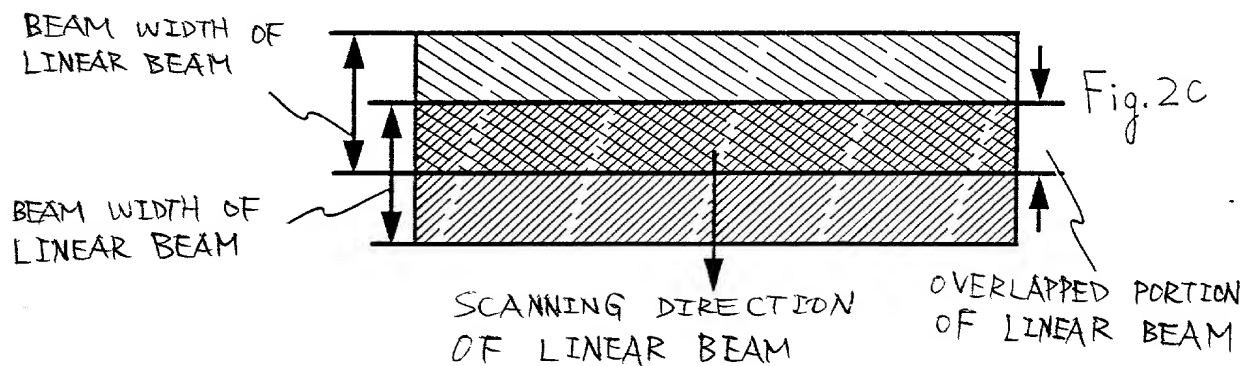
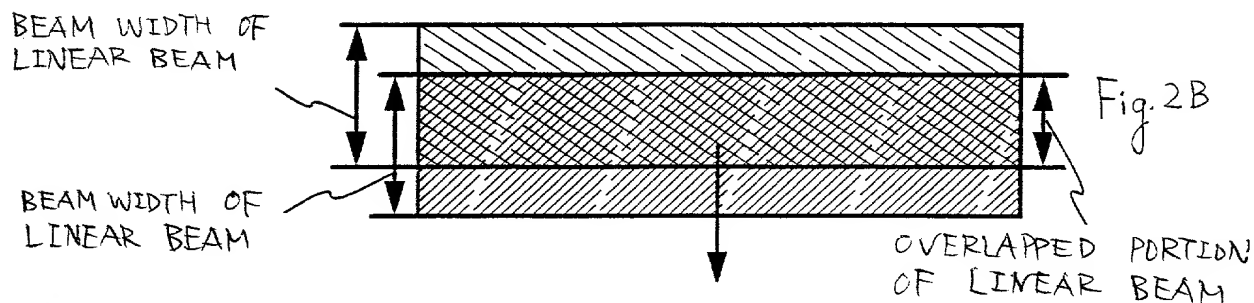
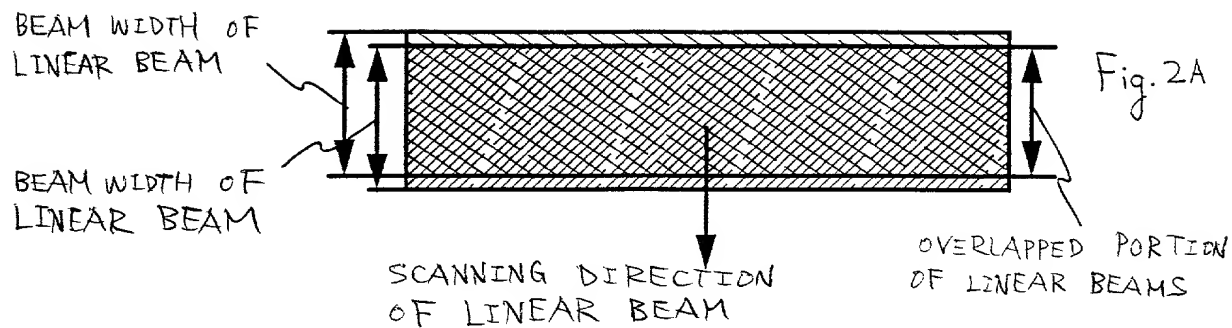


Fig. 3

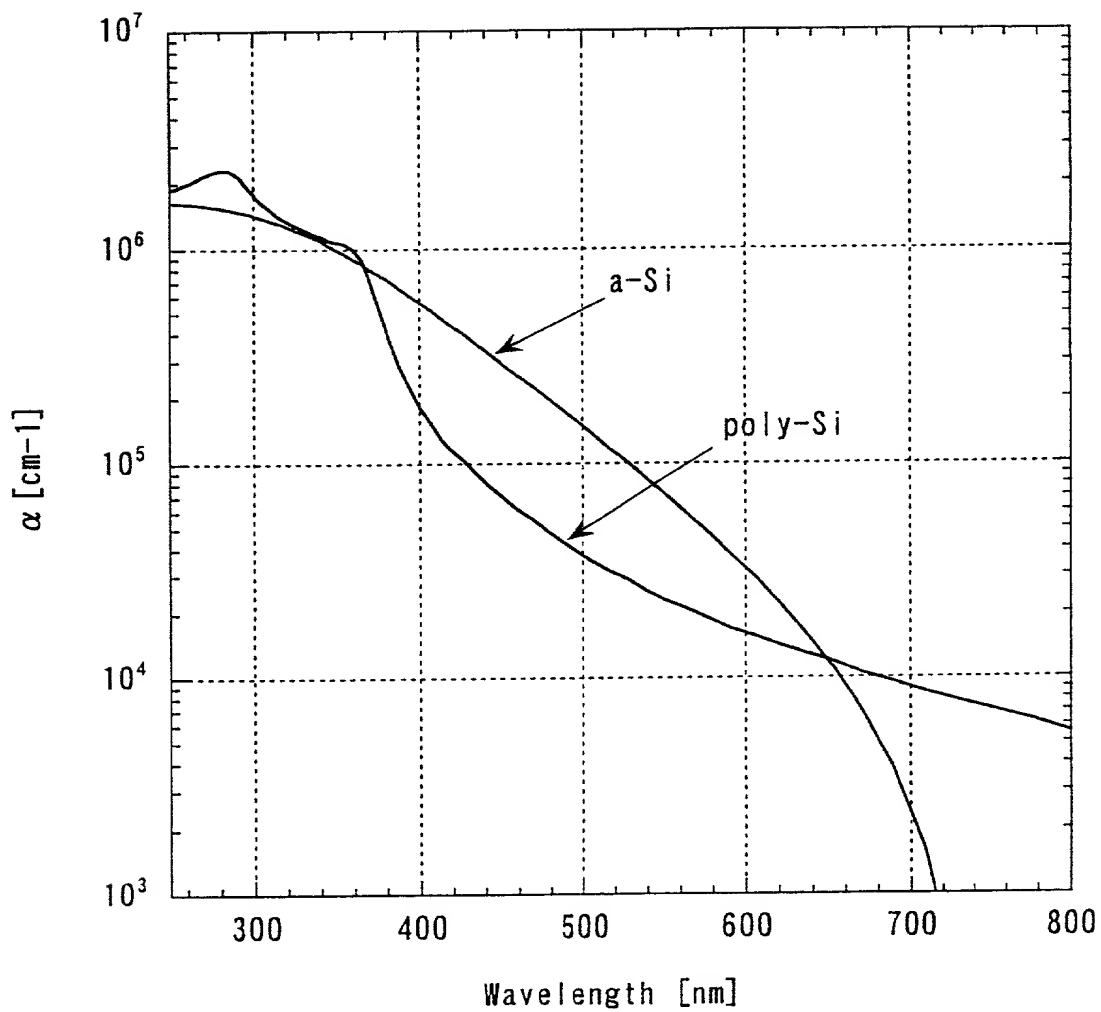


Fig. 4A

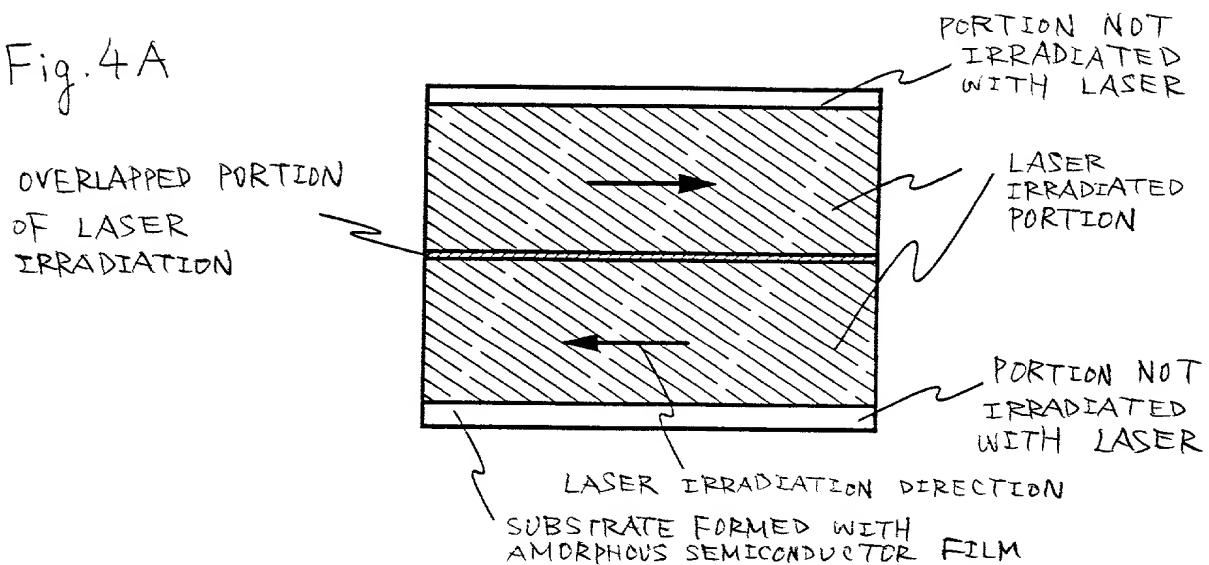


Fig. 4B

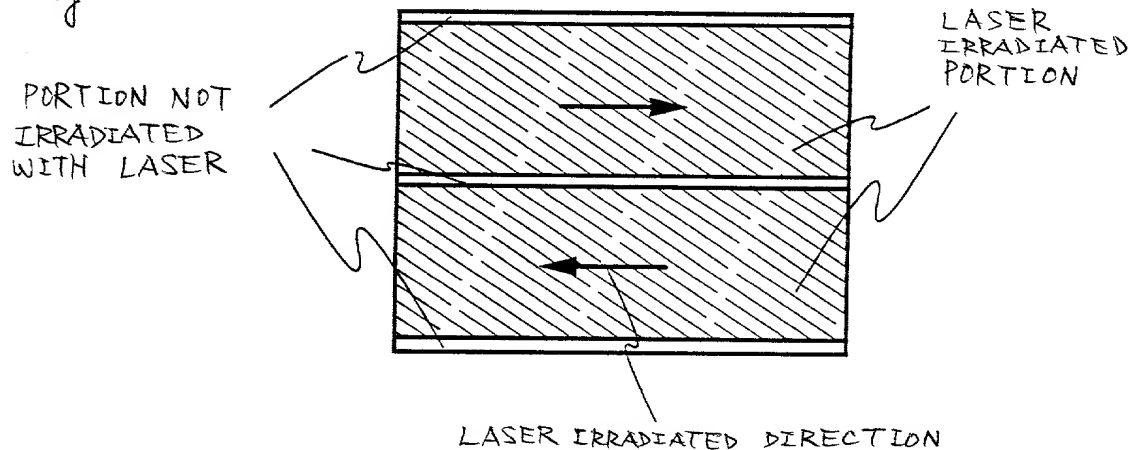


Fig. 4C

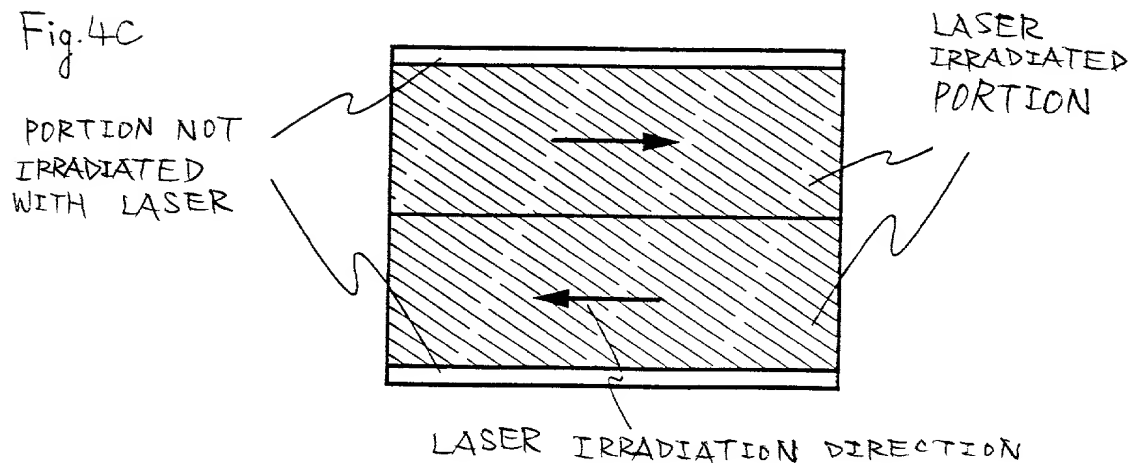


Fig. 5A

SIDE VIEW

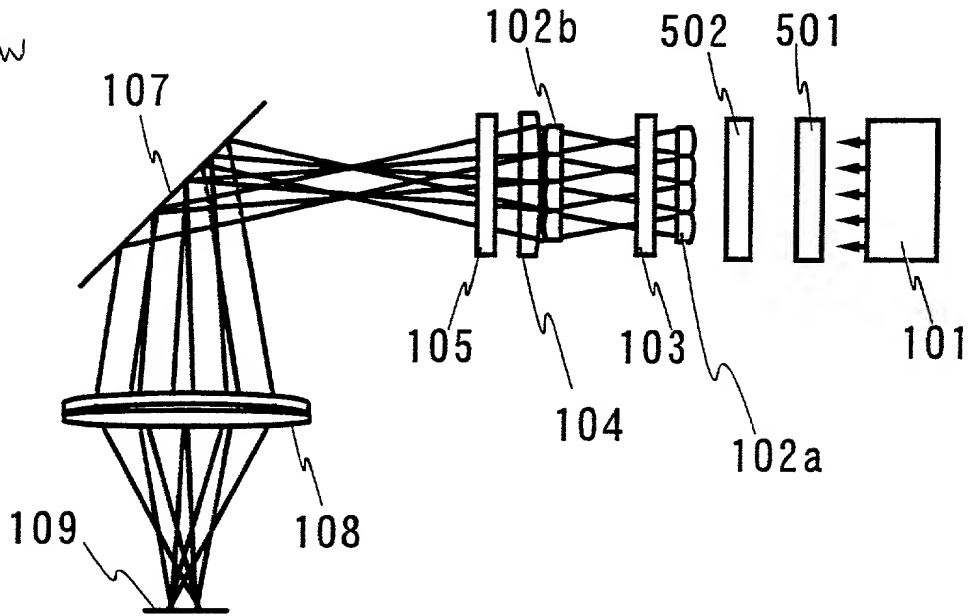


Fig. 5B

PLAN VIEW

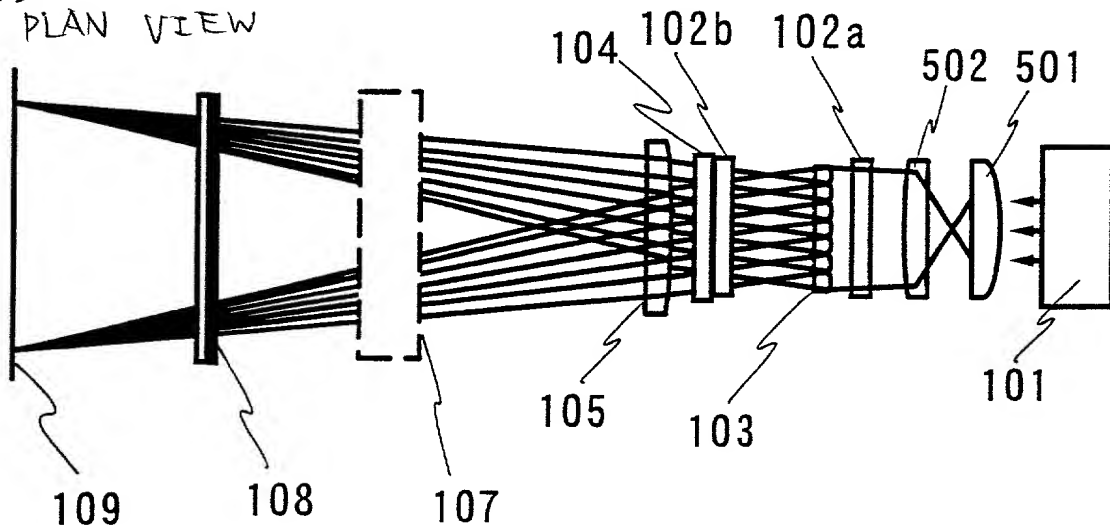
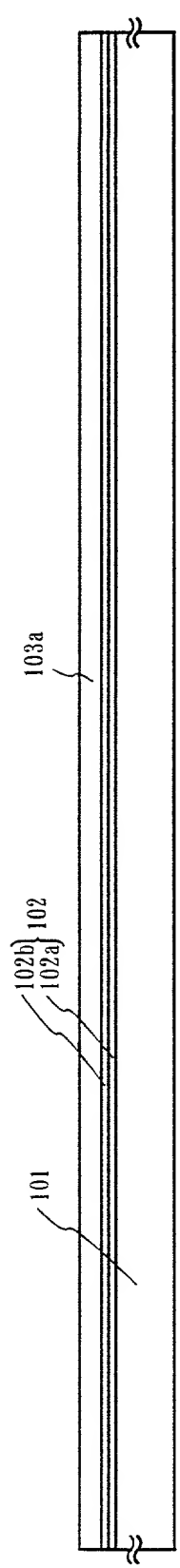


FIG. 6A

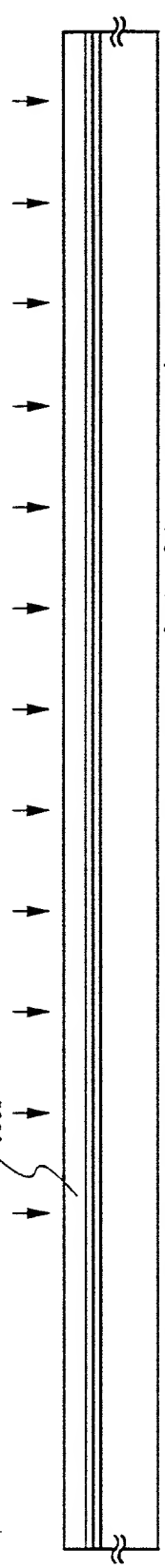
FORMATION OF UNDERLYING FILM AND AMORPHOUS SEMICONDUCTOR FILM

Fig. 6A



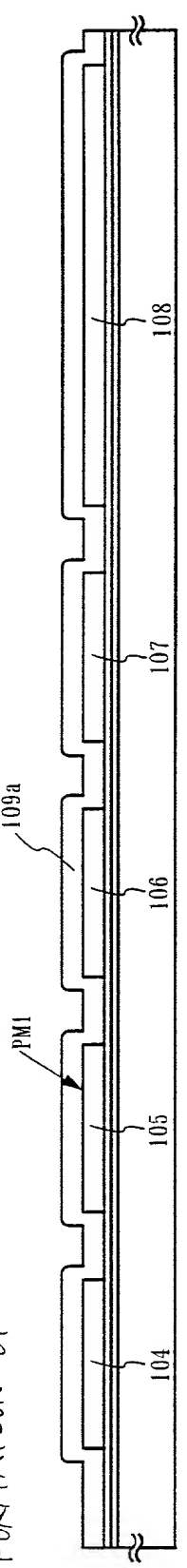
CRYSTALLIZATION PROCESS

Fig. 6B



FORMATION OF ISLAND-SHAPED SEMICONDUCTOR LAYER AND GATE INSULATING FILM

Fig. 6C



FORMATION OF HEAT-RESISTANT CONDUCTIVE LAYER

Fig. 6D

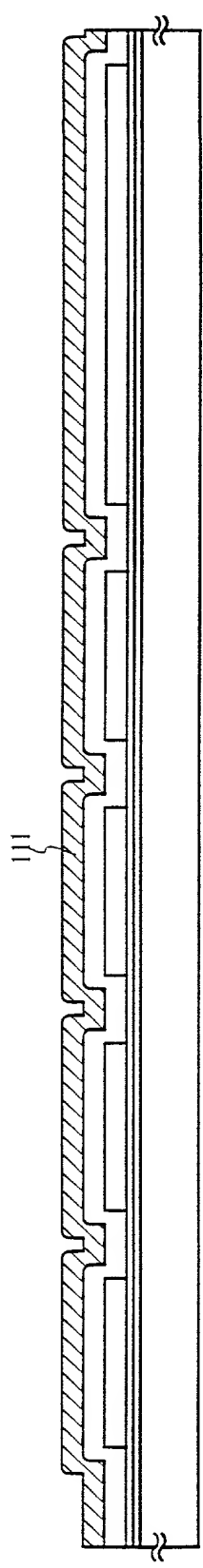


Fig. 7A

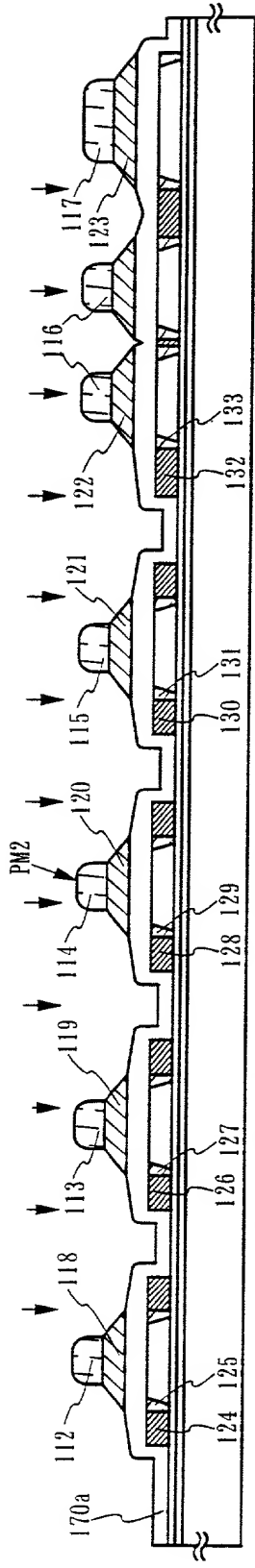


Fig. 7B

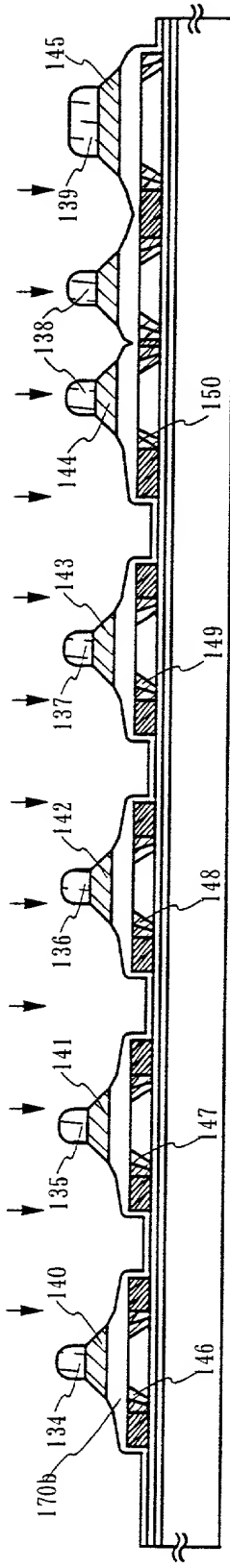


Fig. 7C

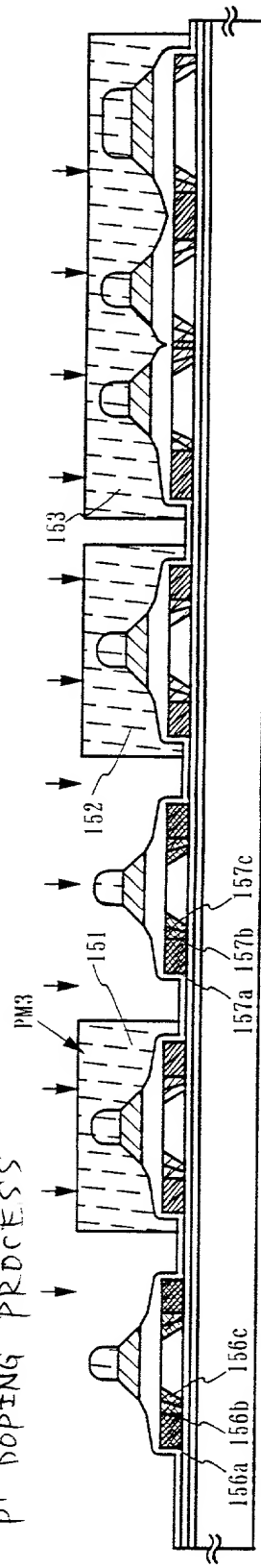
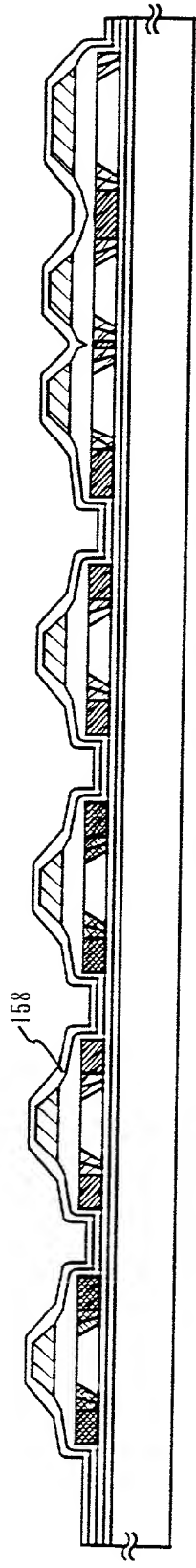


Fig. 8A FORMATION OF FIRST INTERLAYER INSULATING FILM



FORMATION OF SECOND INTERLAYER INSULATING FILM AND CONTACT HOLE

Fig. 8B

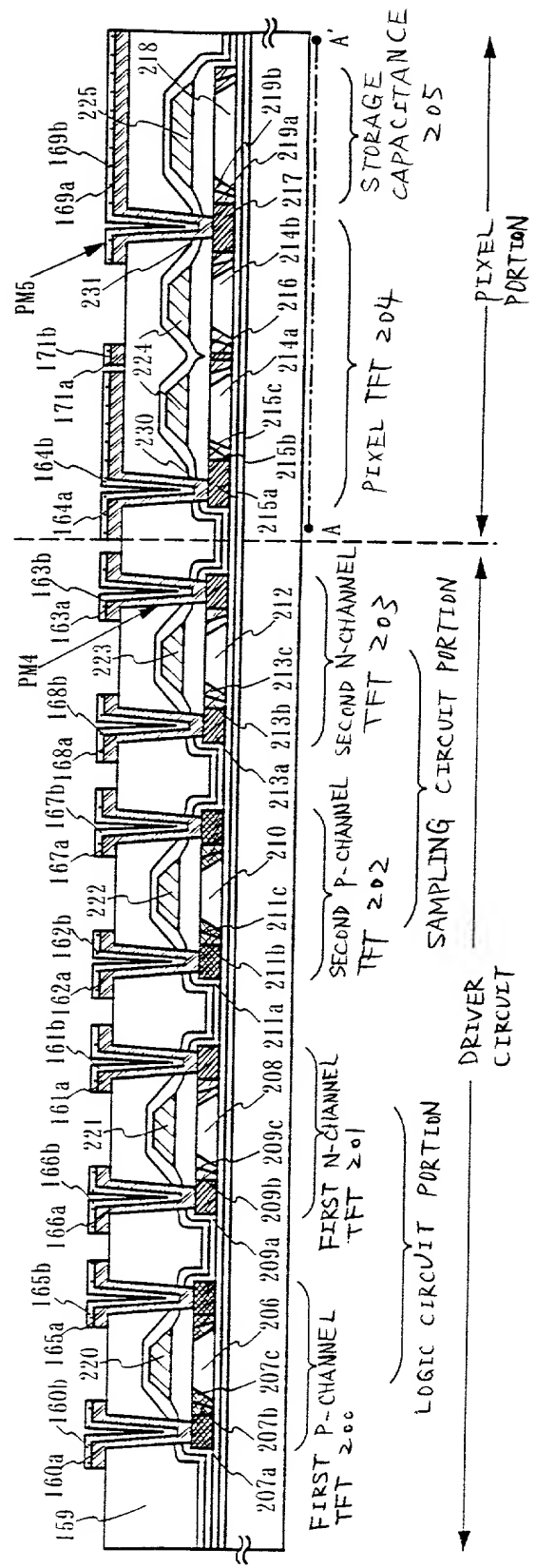
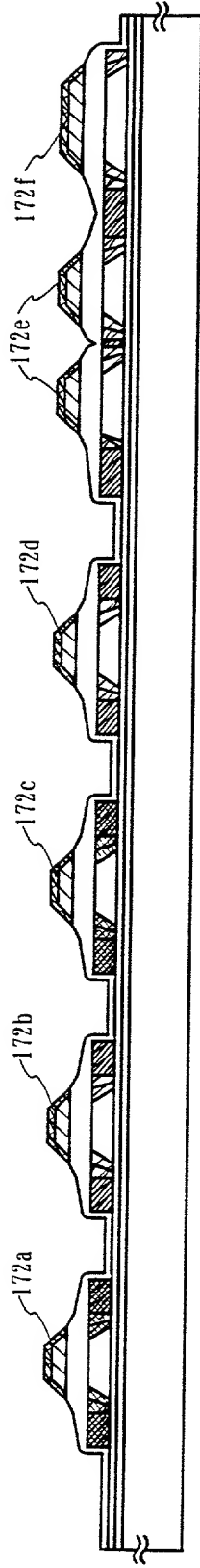
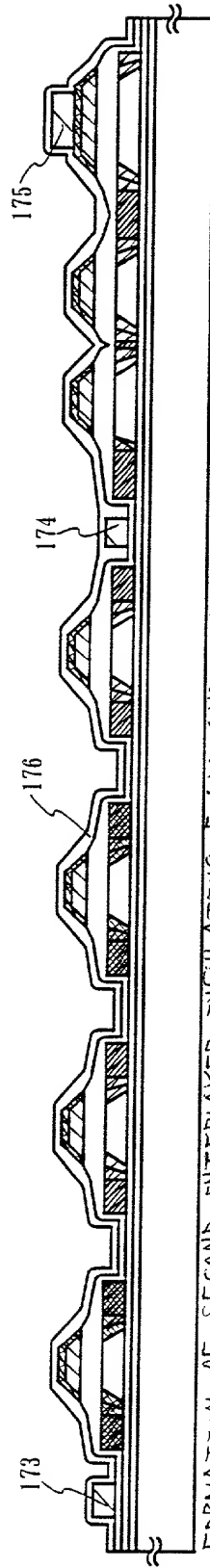


Fig. 9A



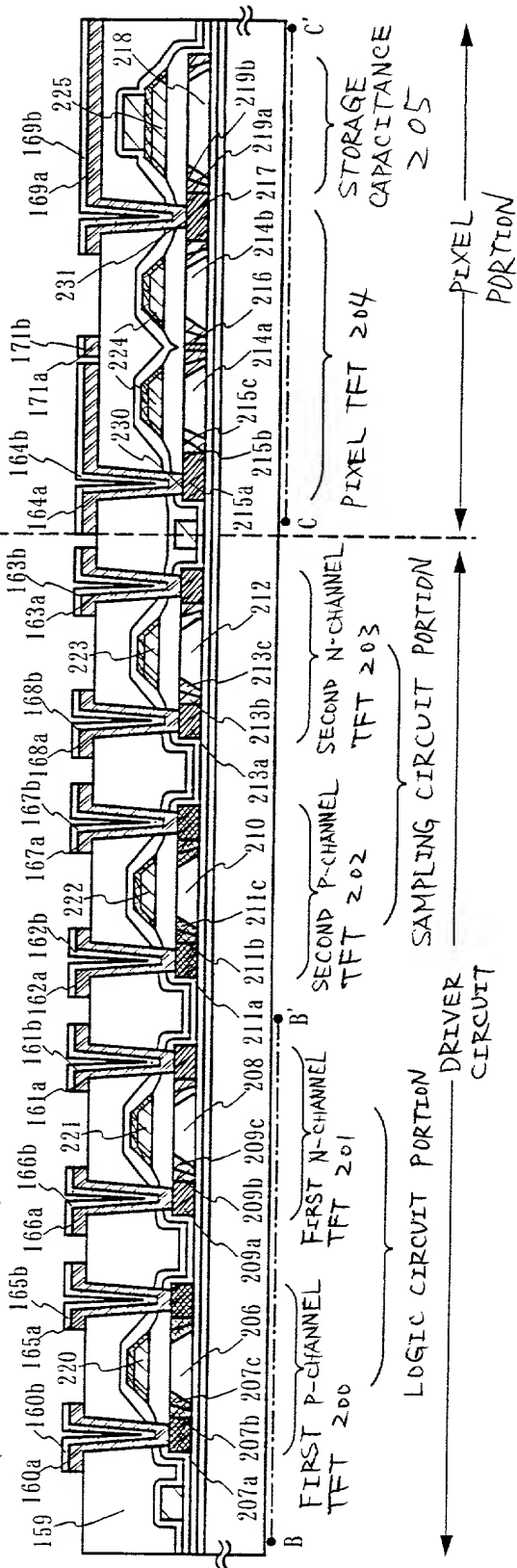
FORMATION OF FIRST INTERLAYER INSULATING FILM

Fig. 9B



FORMATION OF SECOND INTERLAYER INSULATING FILM AND CONTACT HOLE AND WIRING

Fig. 9C



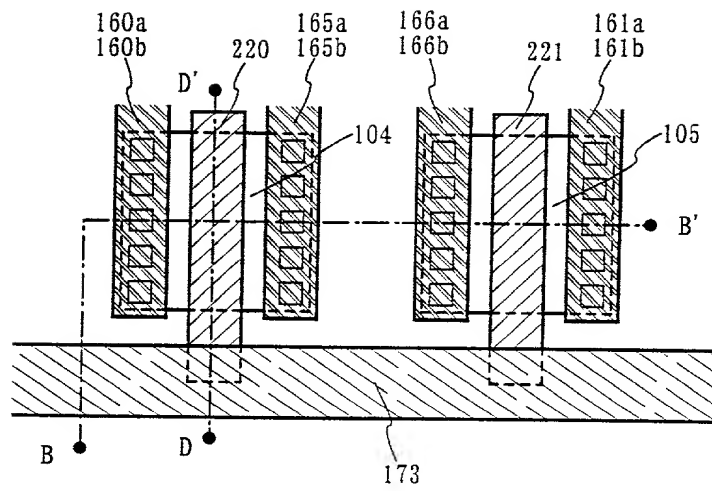


Fig. 10A

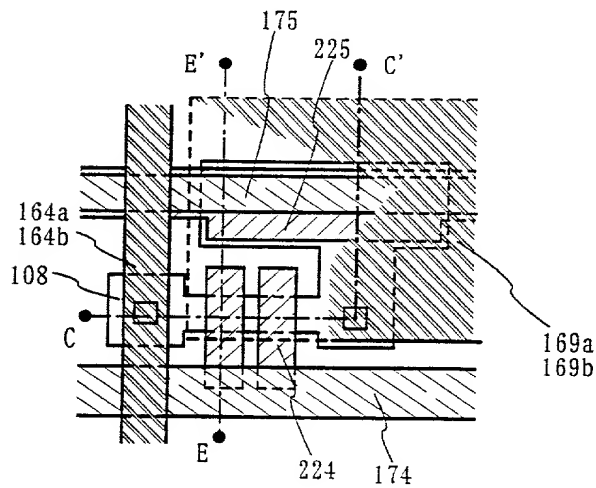


Fig. 10B

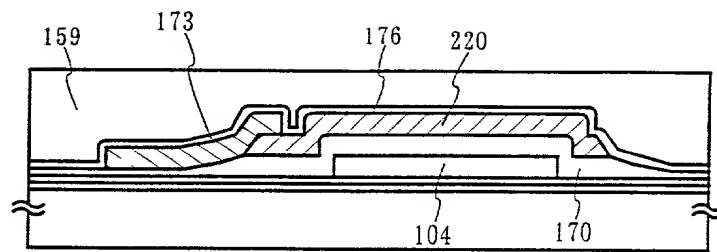


Fig. 11A

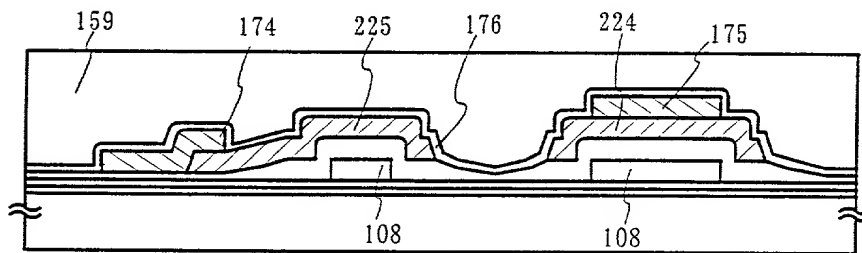
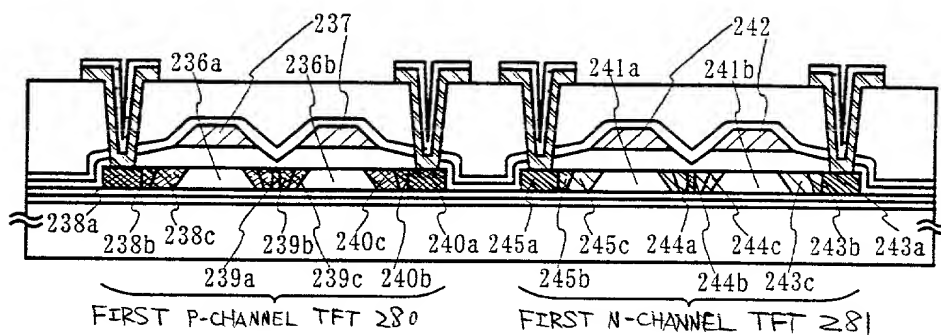
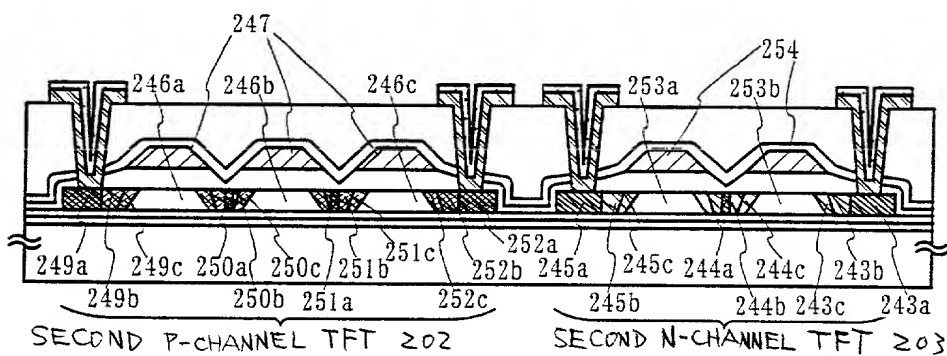


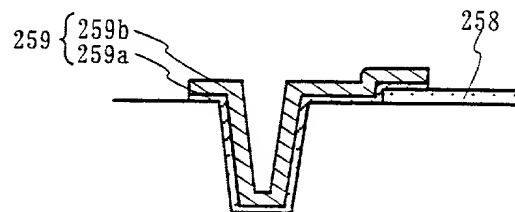
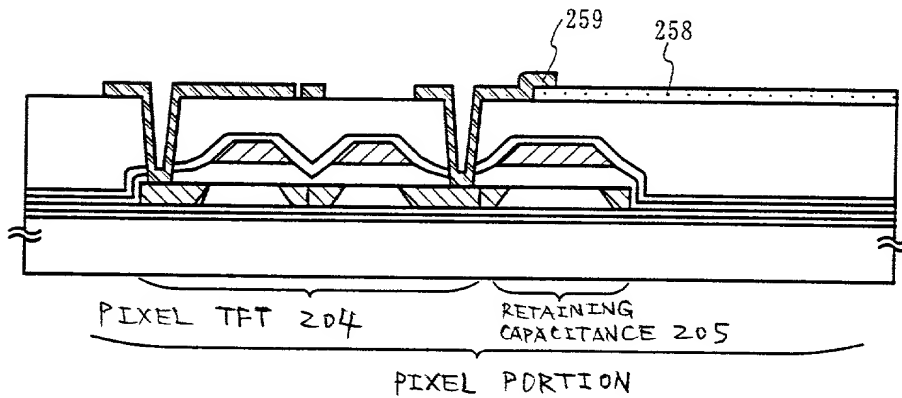
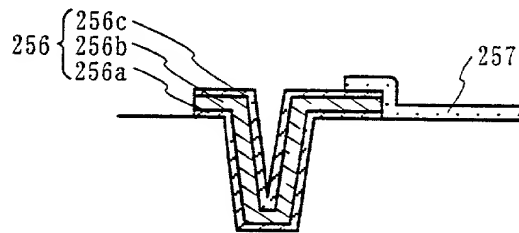
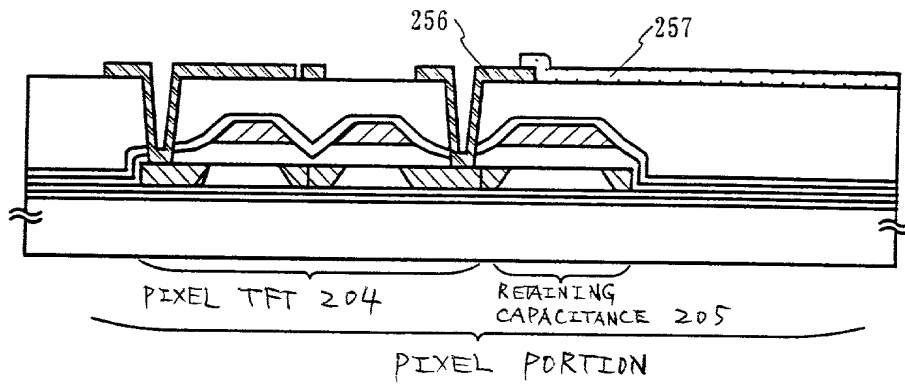
Fig. 11B



LOGIC CIRCUIT PORTION



SAMPLING CIRCUIT PORTION



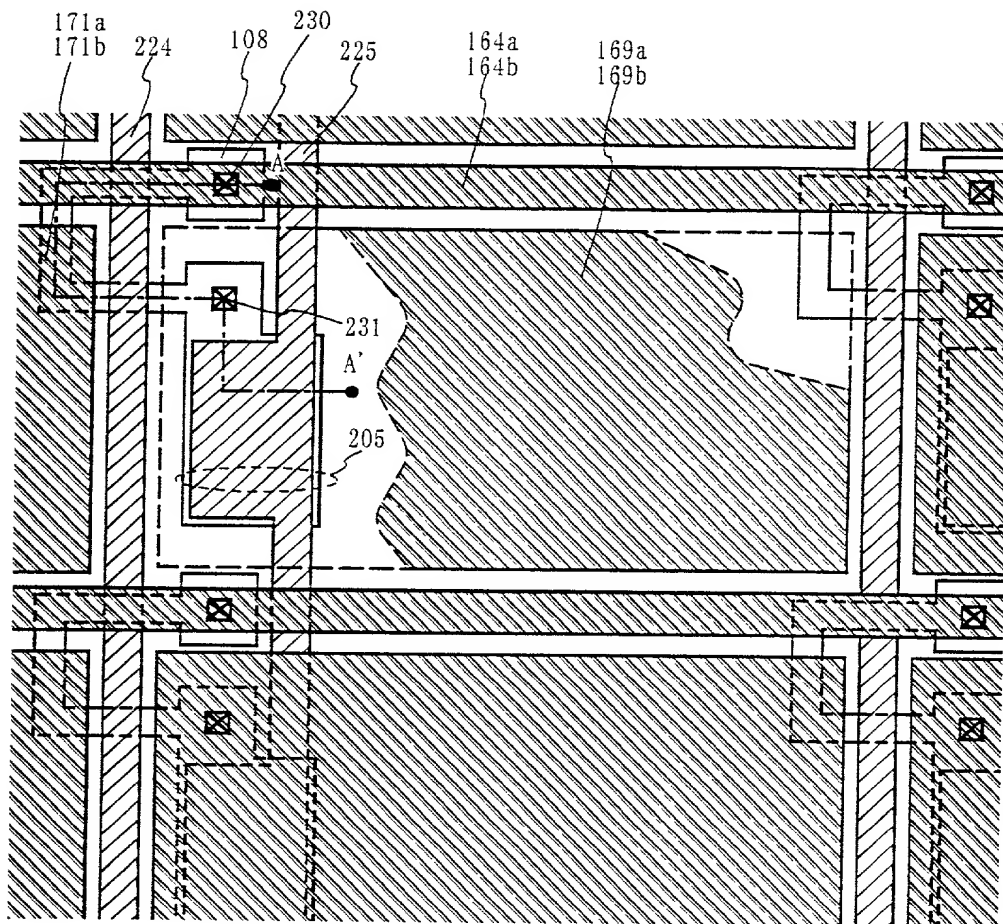


Fig. 14

FIG. 15A is a cross-sectional view of a pixel portion of a display device. The pixel portion includes a first p-channel TFT 200, a first n-channel TFT 201, a second p-channel TFT 202, a second n-channel TFT 203, a storage capacitor 205, and a pixel electrode 231. The pixel portion is connected to a driver circuit and a sampling circuit. The driver circuit includes a first p-channel TFT 200 and a first n-channel TFT 201. The sampling circuit includes a second p-channel TFT 202 and a second n-channel TFT 203. The storage capacitor 205 is connected to the second n-channel TFT 203 and the pixel electrode 231. The pixel electrode 231 is connected to the second p-channel TFT 202 and the second n-channel TFT 203. The pixel portion is connected to a data line 406 and a gate line 407. The data line 406 is connected to the pixel electrode 231. The gate line 407 is connected to the gate of the first p-channel TFT 200 and the gate of the first n-channel TFT 201. The pixel portion is connected to a common data line 408 and a common gate line 409. The common data line 408 is connected to the pixel electrode 231. The common gate line 409 is connected to the gate of the second p-channel TFT 202 and the gate of the second n-channel TFT 203.

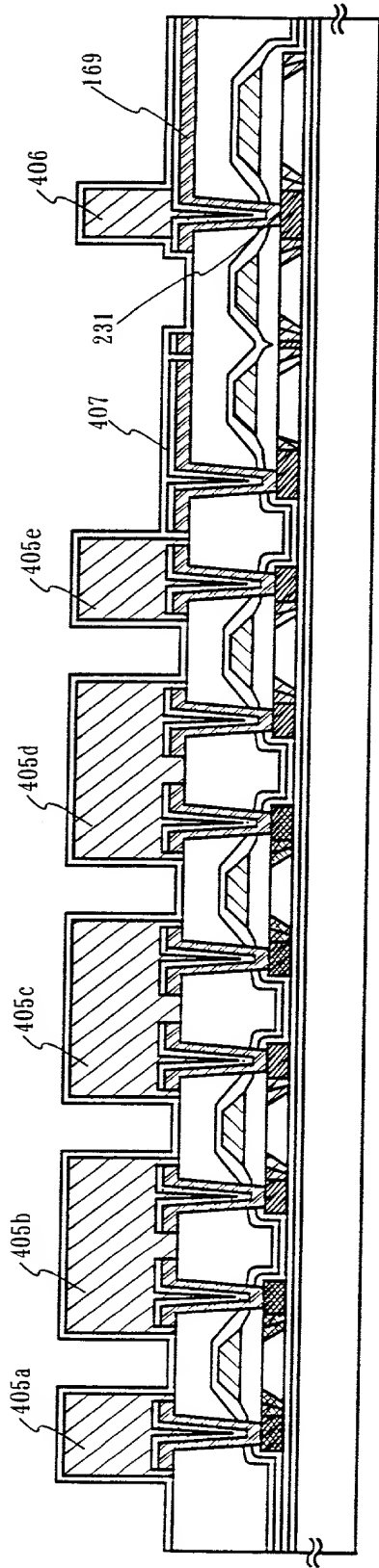


Fig. 15A

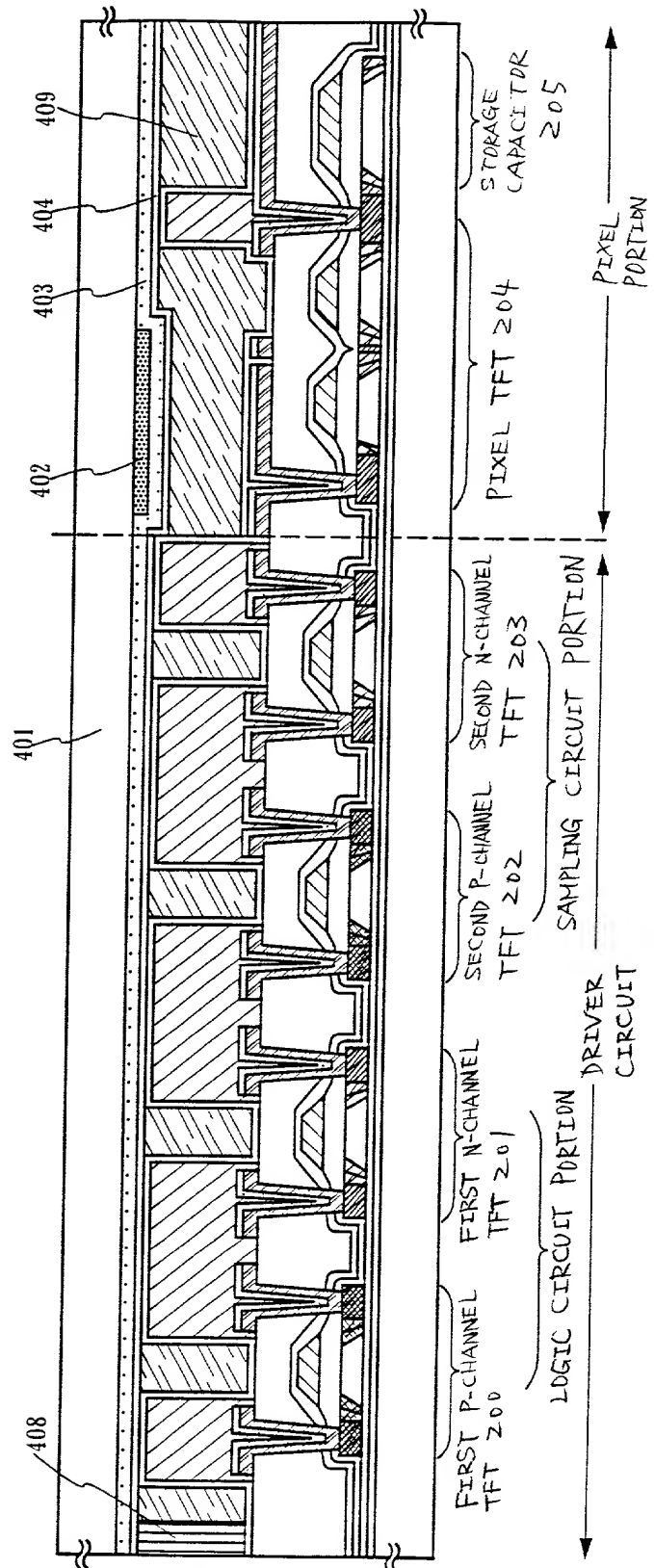


Fig. 15B

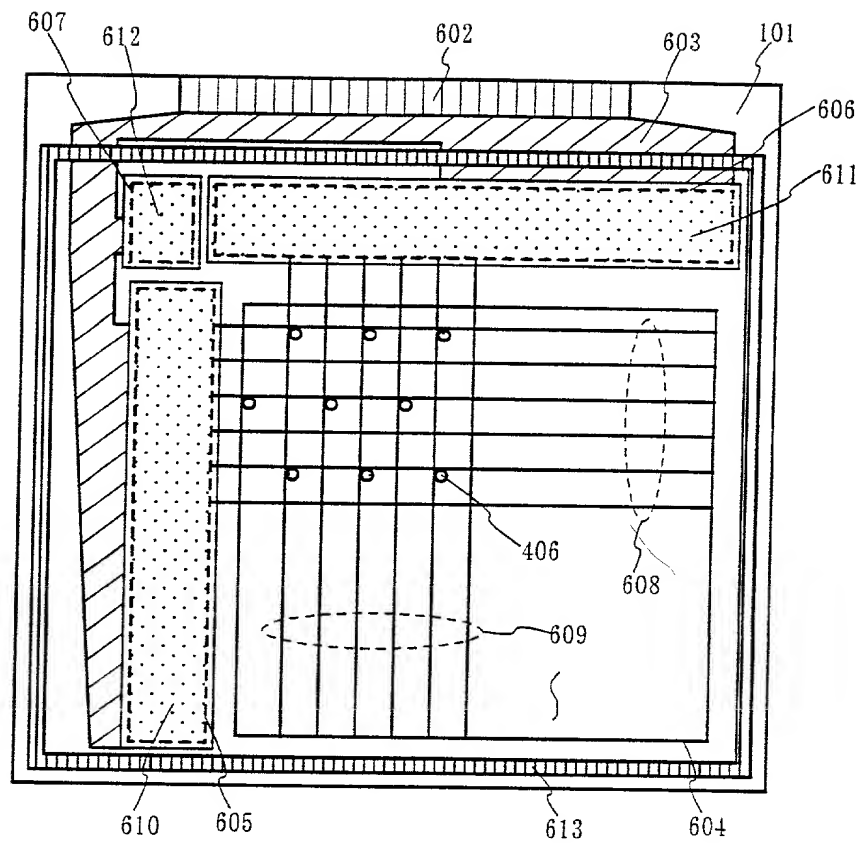


Fig. 16

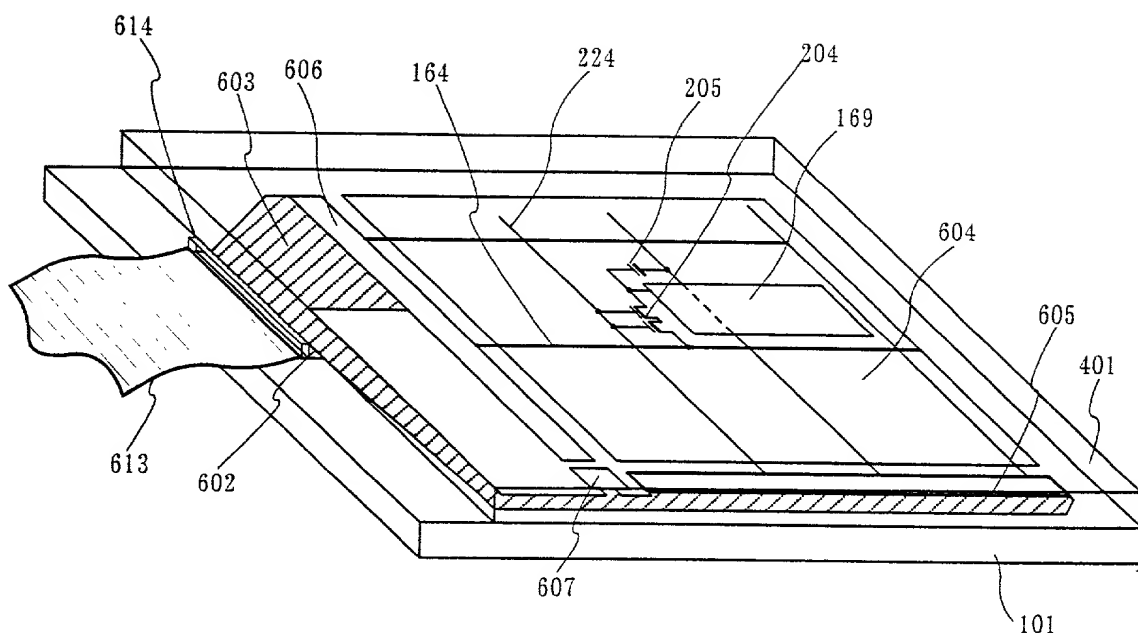


Fig. 17

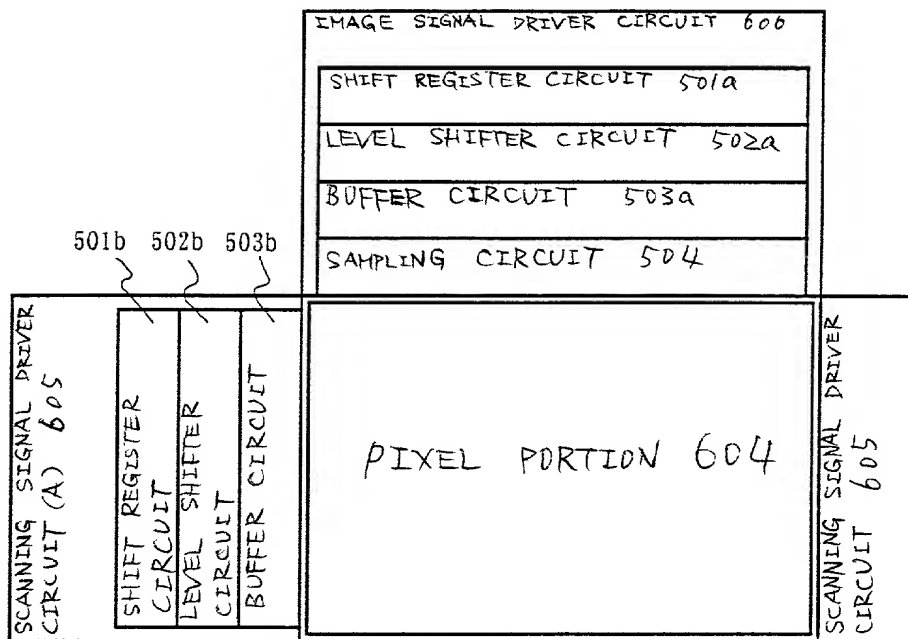


Fig. 18

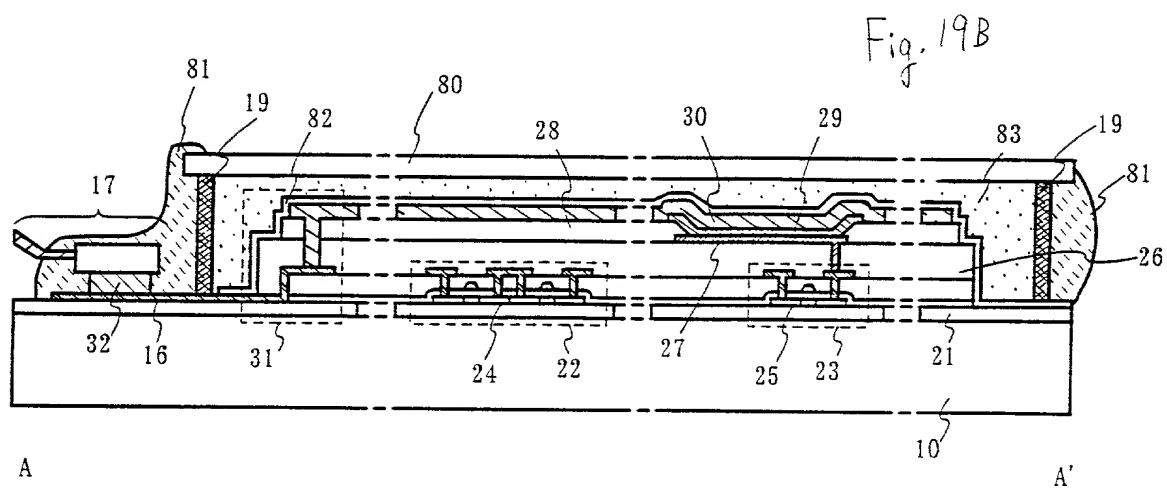
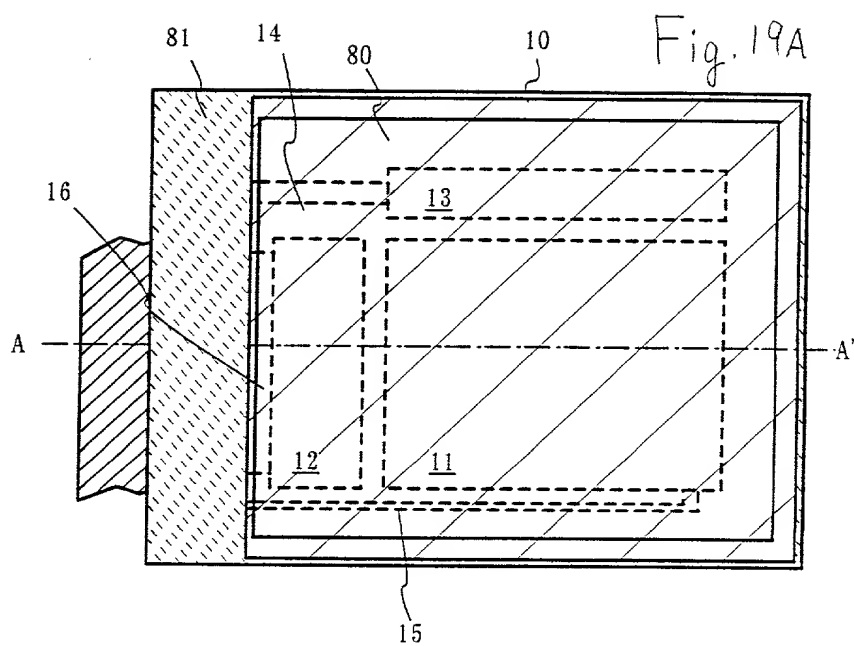


FIG. 20A is a cross-sectional view of a pixel structure in a first embodiment of the present invention. The pixel structure includes a switching TFT 2402, an EL element 2405, and a current controlling TFT 2403. The switching TFT 2402 includes a gate 36, a source 35, and a drain 38. The EL element 2405 is connected to the source 35 of the switching TFT 2402 and includes a cathode 44a, an emission layer 45, and an anode 46. The current controlling TFT 2403 includes a gate 40, a source 41, and a drain 42. The gate 40 of the current controlling TFT 2403 is connected to the anode 46 of the EL element 2405. The source 41 of the current controlling TFT 2403 is connected to the drain 38 of the switching TFT 2402. The drain 42 of the current controlling TFT 2403 is connected to a power supply 48. The pixel structure is formed on a substrate 2401.

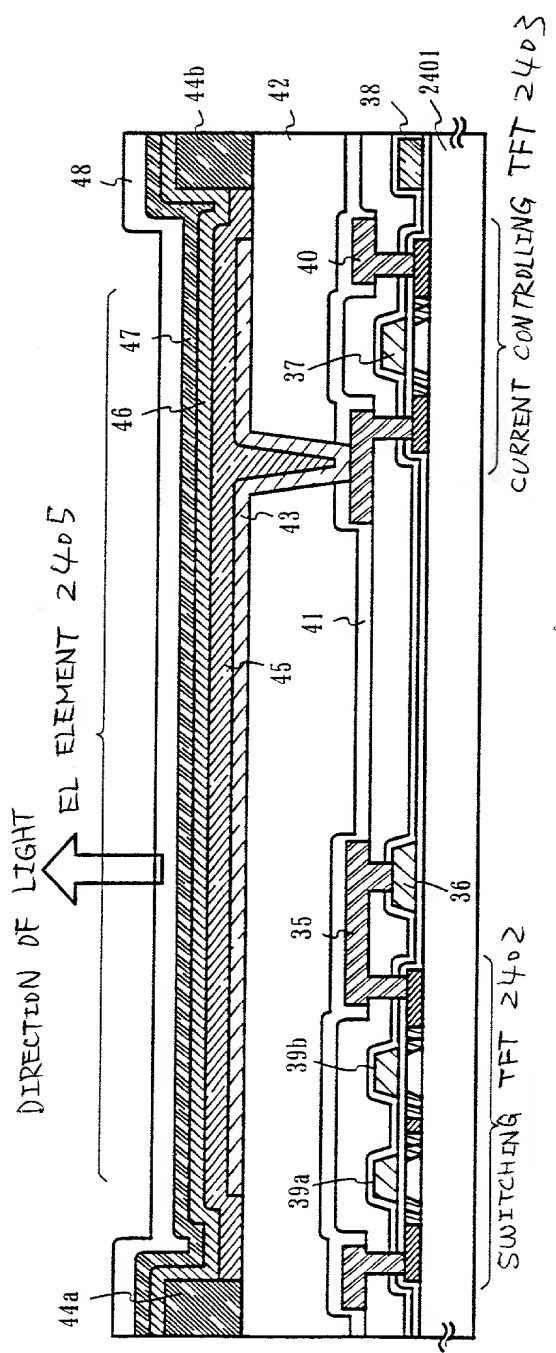
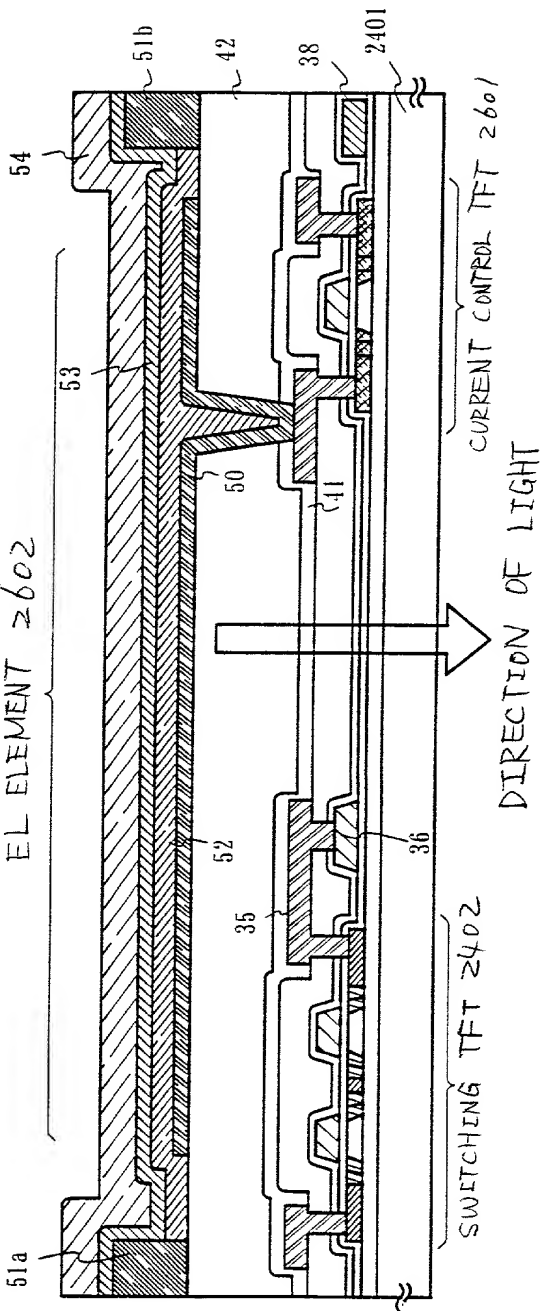
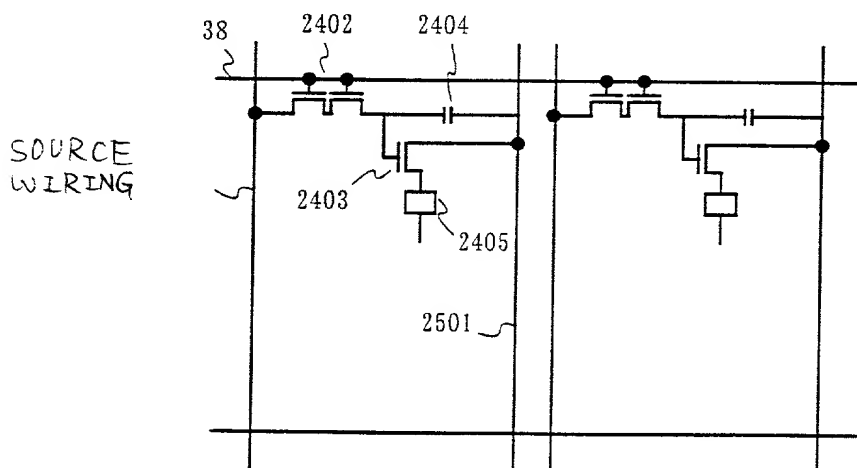
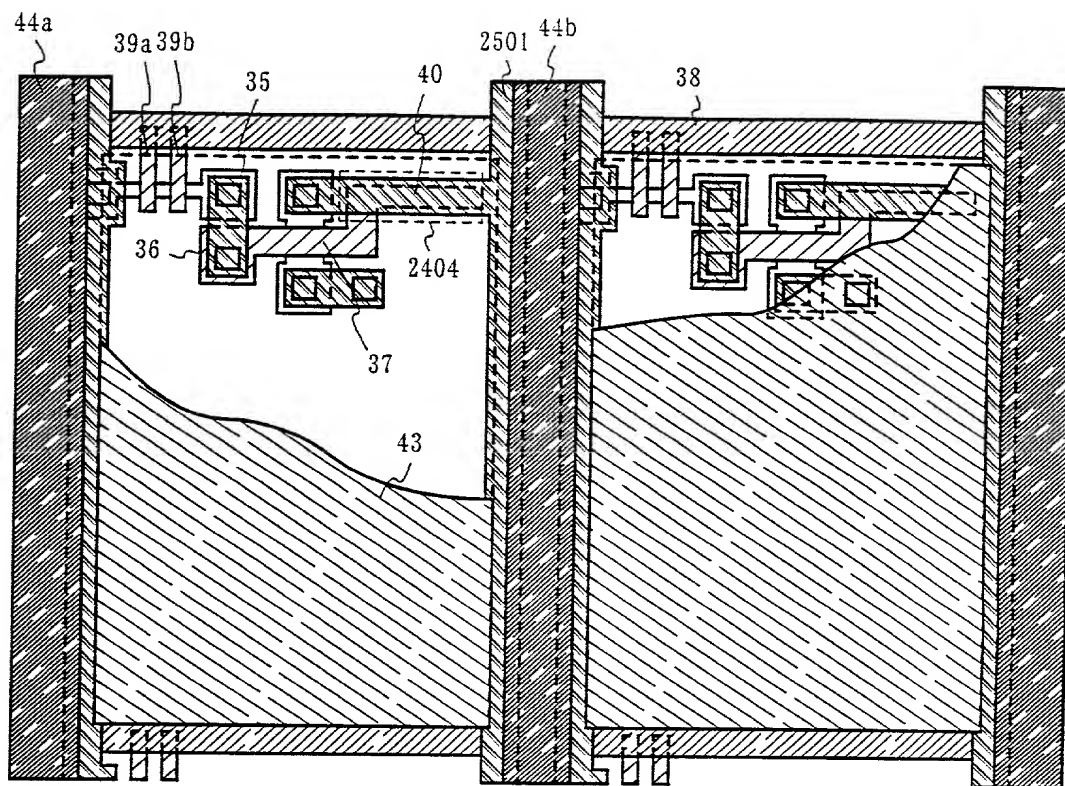


Fig. 20B





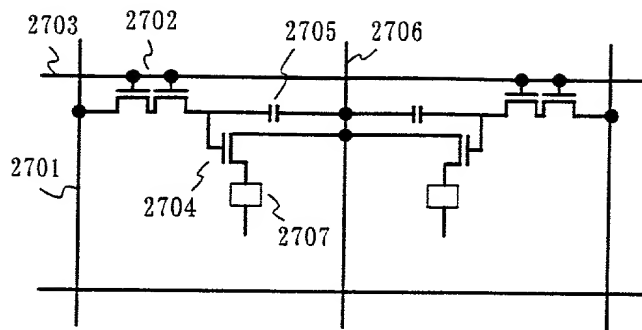


Fig. 22A

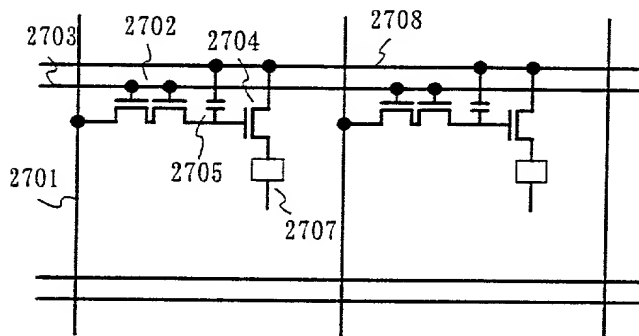


Fig. 22B

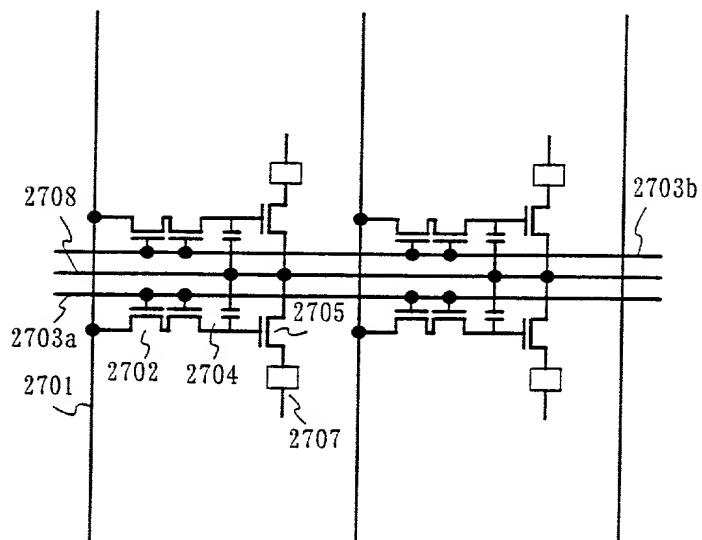


Fig. 22C

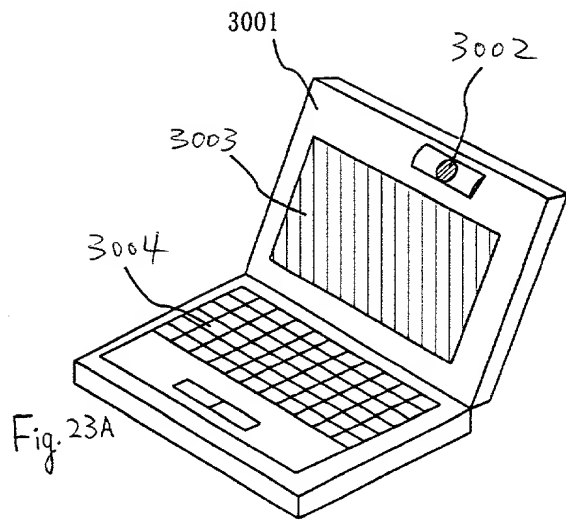


Fig. 23A

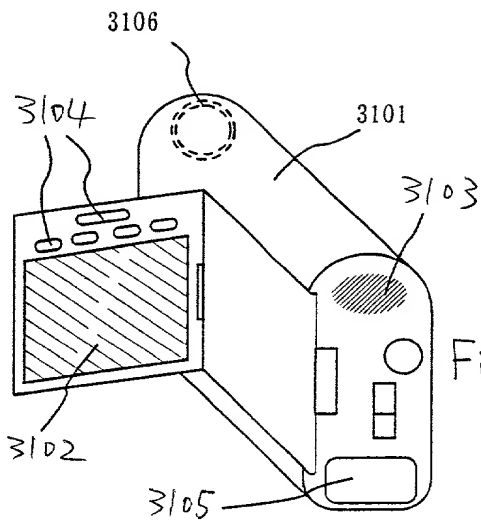


Fig. 23B

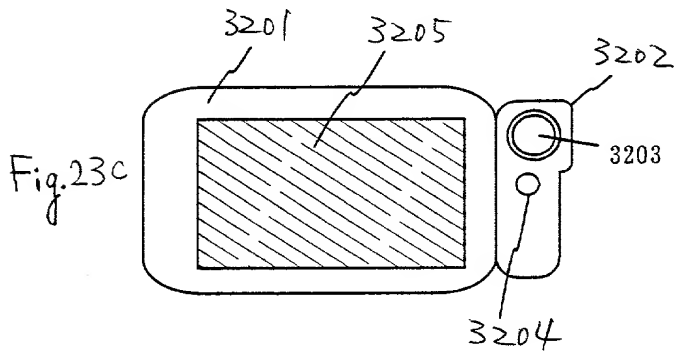


Fig. 23C

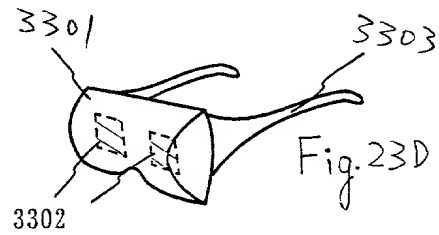


Fig. 23D

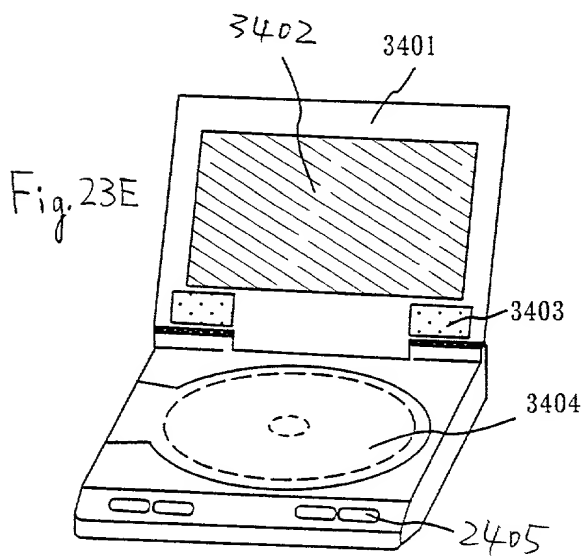


Fig. 23E

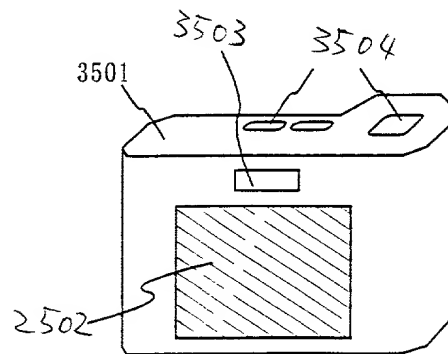


Fig. 23F

FIG. 23A is a perspective view of a laptop computer. FIG. 23B is a perspective view of a handheld device. FIG. 23C is a perspective view of a handheld device. FIG. 23D is a perspective view of a handheld device. FIG. 23E is a perspective view of a handheld device. FIG. 23F is a perspective view of a handheld device.

Fig. 24A

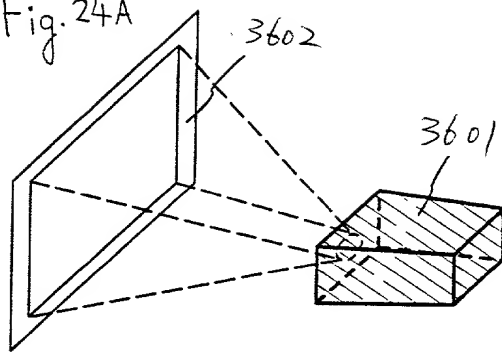


Fig. 24B

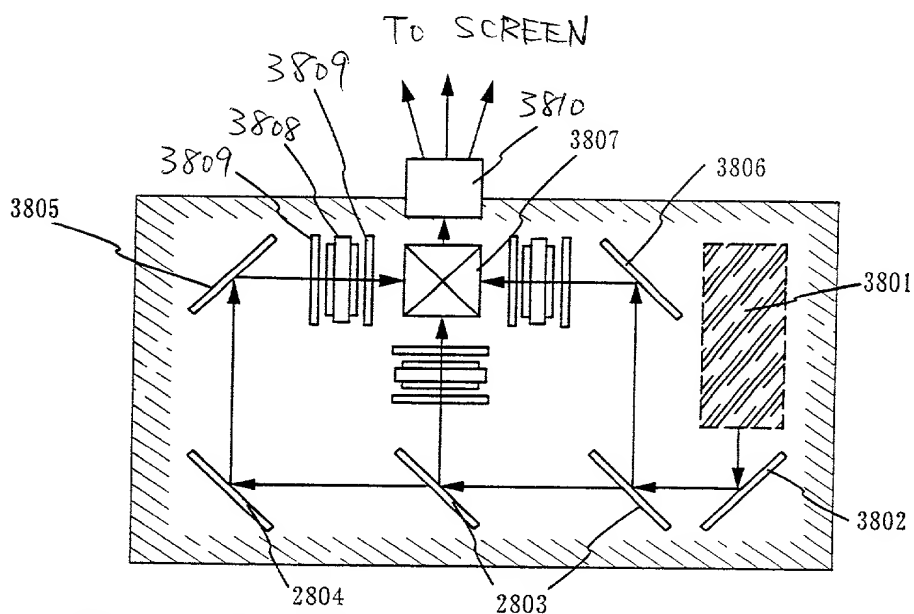
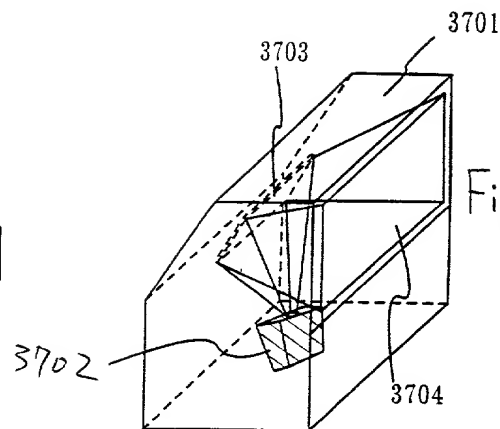


Fig. 24C PROJECTION DEVICE (THREE PLATE TYPE)

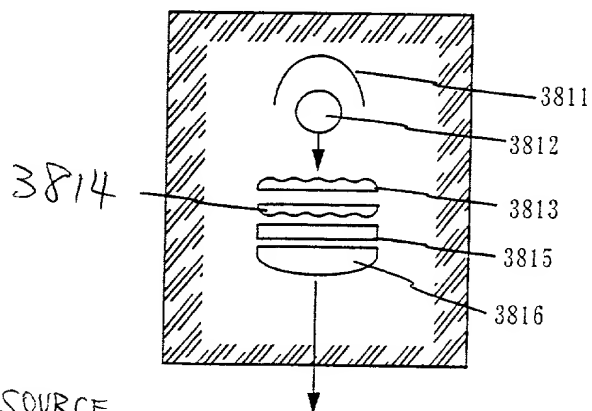


Fig. 24D LIGHT SOURCE OPTICAL SYSTEM

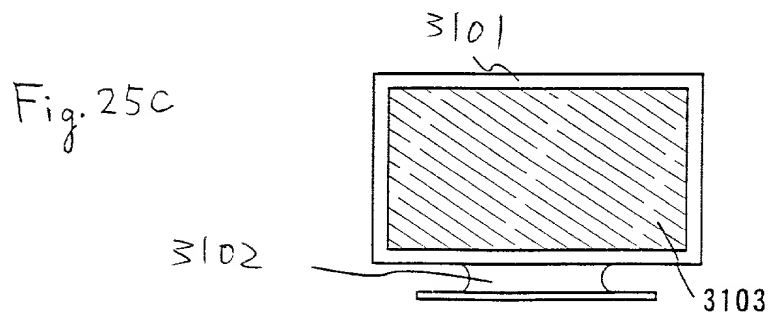
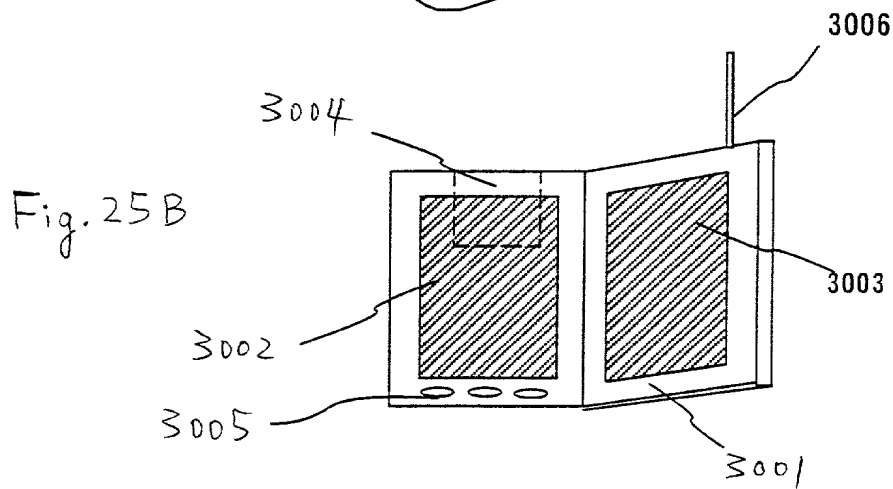
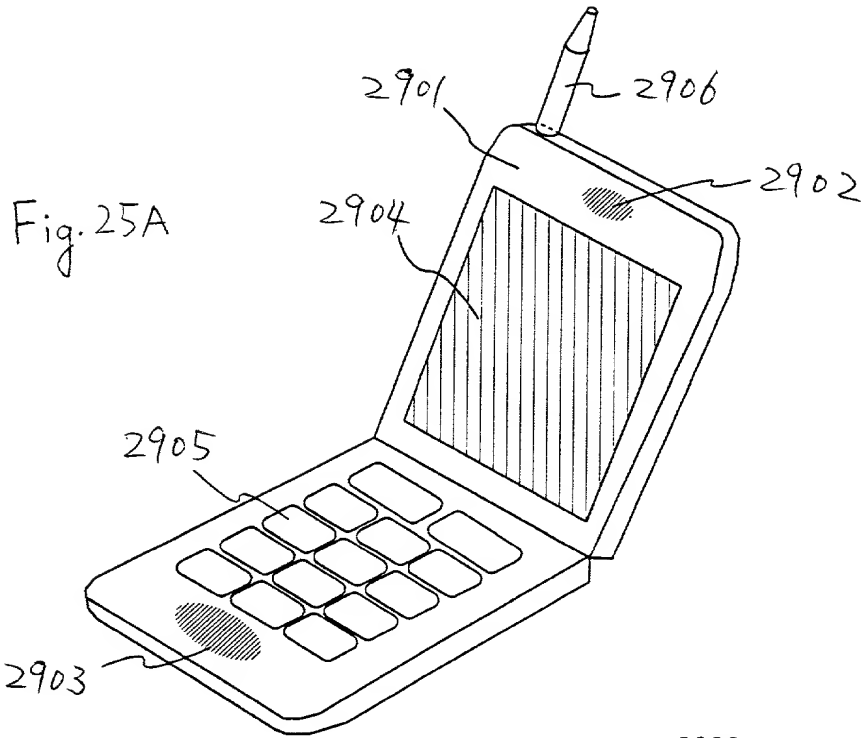


Fig. 26A

OVERLAPPED PORTION
OF LASER
IRRADIATION

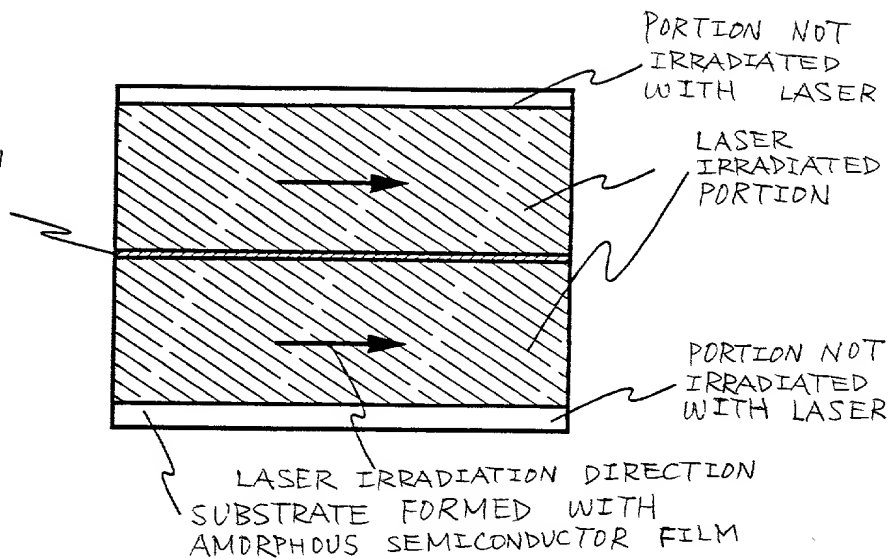


Fig. 26B

PORTION NOT
IRRADIATED
WITH LASER

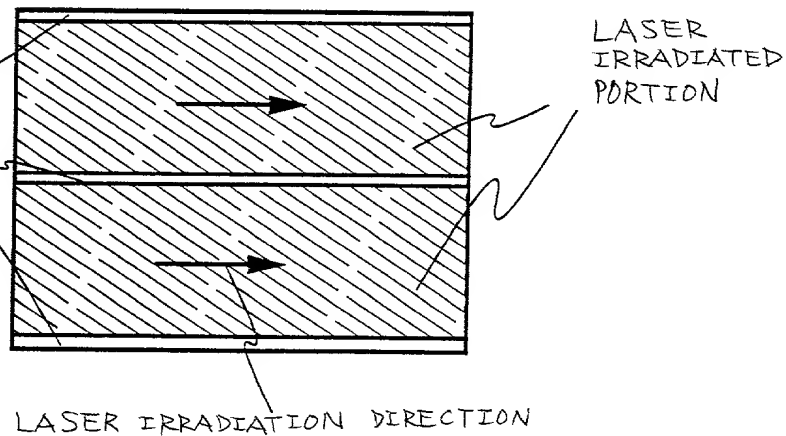


Fig. 26C

PORTION NOT
IRRADIATED
WITH LASER

